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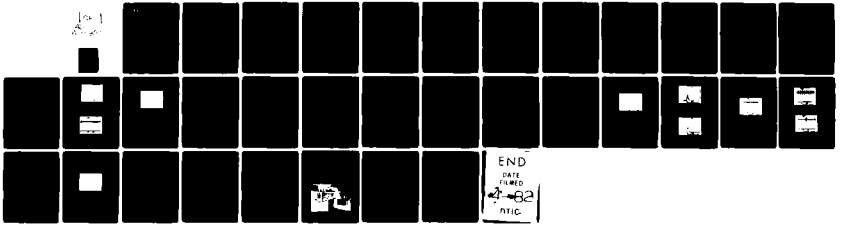

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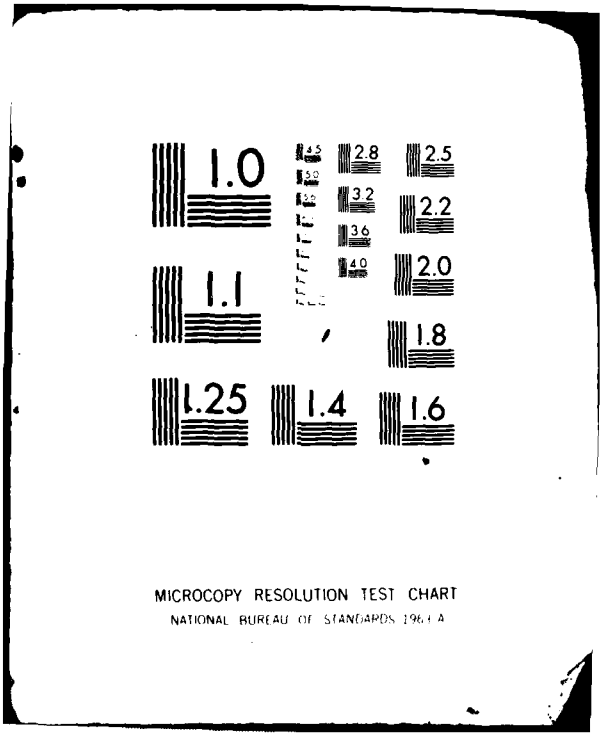
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RESEARCH AND DEVELOPMENT TECHNICAL REPORT

DELEW-TR- 82-1

ANGLE OF ARRIVAL PHASE INTERFEROMETER DIRECTION FINDING SYSTEM

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JANUARY 1982

ERADCOM

US ARMY ELECTRONICS RESEARCH & DEVELOPMENT COMMAND
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This technical report describes an angle of arrival phase interferometer direction finding system using a dual channel SAW compressive receiver and extensive digital processing.

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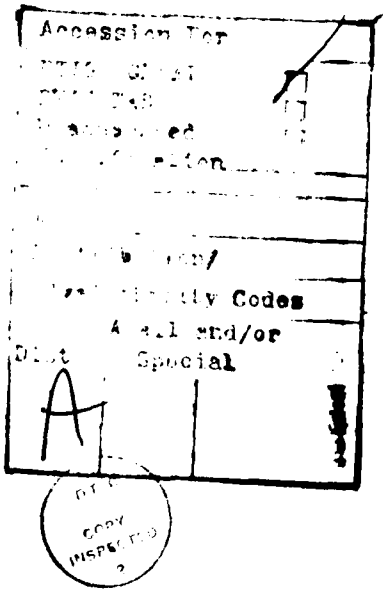


ANGLE OF ARRIVAL PHASE INTERFEROMETER DIRECTION FINDING SYSTEM

by

Charles Konig
William Skudera

INTRODUCTION

Many US Army Direction Finding Systems, now fielded or in development, are narrowband systems that will not be capable of handling the high pulse data throughputs in the late 1980's or 1990's. This report describes a high throughput direction finding (DF) system whose technology will make it possible to thwart future threats. Radar signal processors capable of handling millions of pulses per second will be required to handle many exotic emitters. This report describes the techniques and technology needed for such a high speed signal processor.

DISCUSSION

a. Review of Phase Interferometer

Some electronic warfare (EW) applications require line-of-bearing (LOB) information on a particular emitter or on a number of emitters. The two most common techniques are the amplitude comparison and the phase interferometer.

Figure 1 illustrates the basic geometric relationships governing a simple phase interferometer. The operating bandwidth of an interferometer is usually restricted to one octave, which is a two-to-one ratio in frequency.

$$\theta = \frac{\lambda}{2\pi d} \sin^{-1}\phi \qquad (1)$$

θ = angle of arrival (AOA) in degrees
λ = wavelength in meters
d = antenna seperation in λ meters
$2\pi = 360^0$ = constant value
ϕ = electrical phase angle in degrees

No ambiguities exist as long as the antenna baseline is less than $\frac{d}{2}$.

The phase interferometer configuration provides the system designer with the geometry to obtain an emitter AOA. The first step in this implementation is to translate the electromagnetic field on the antennas into an electrical phase angle measurement ϕ.

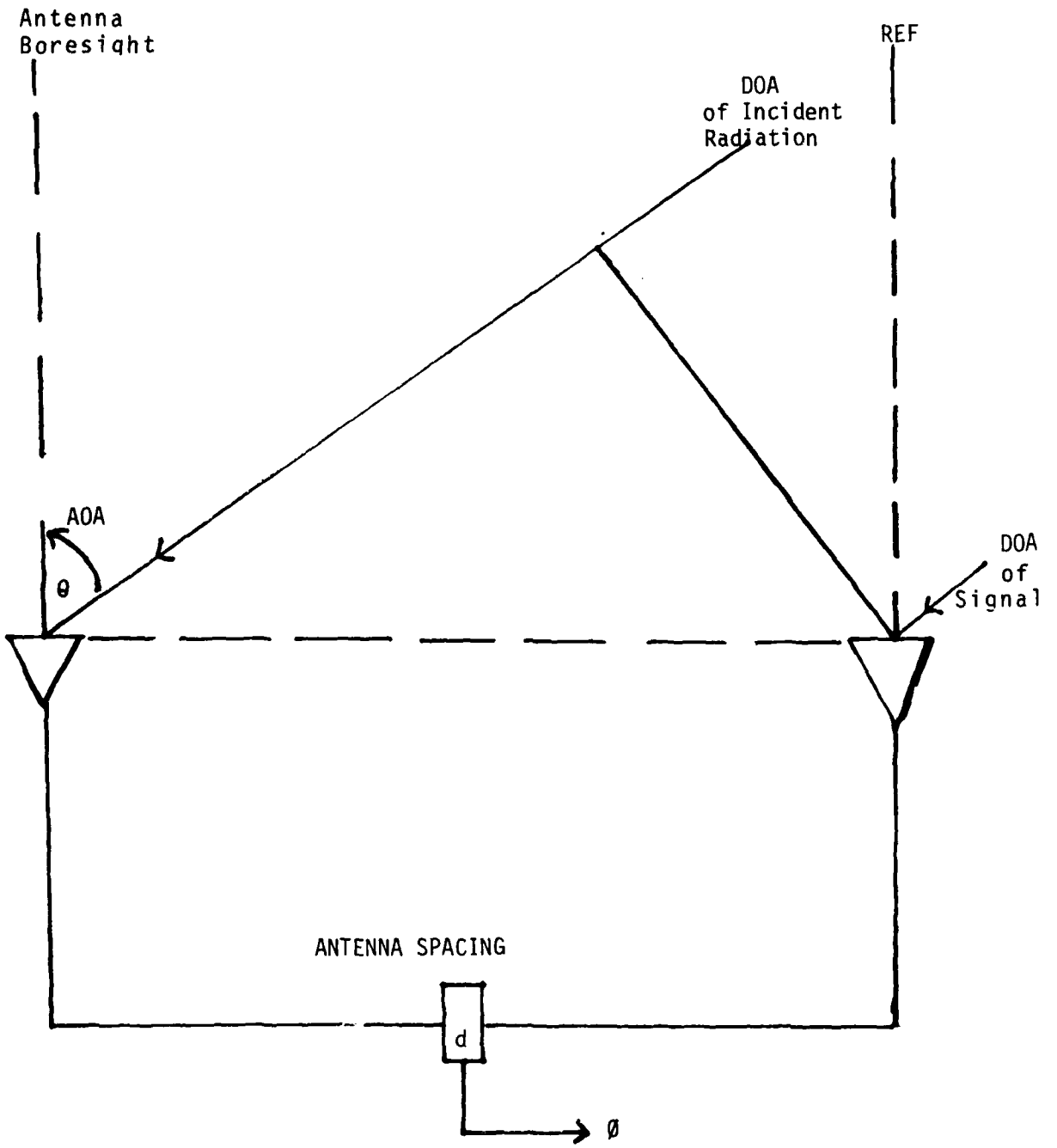


Figure 1. Phase interferometer baseline.

$$\phi = \tan^{-1} \frac{Q}{I} \qquad (2)$$

where

ϕ = electrical phase angle
Q = quadrature component
I = in-phase component. (3)

The in-phase and quadrature components are derived from a phase comparator which is located in the radio frequency (RF) receiver. The phase comparator is a passive four port network capable of resolving the phase difference between RF signals of the same identical frequency. When two signals of electrical phase differences are applied to the unknown RF and reference local oscillator (LO) ports respectively, two demodulated outputs result. The "X" output is a voltage proportional to the cosine of this phase difference, and the "Y" output is proportional to the sine.

$$E_x = KE_x \cos \phi$$

$$E_y = KE_y \sin \phi$$

$$\tan \phi = \frac{E_y}{E_x} \qquad (4)$$

E_x, E_y are the output voltages

E is the input voltage

K is a constant of conversion (demodulation efficiency)

An important feature to be noted from the above relationships is that phase comparisons can be made uniquely over a 0^0 - 360^0 phase difference range.

Basically, the phase comparator is an integrated assembly of a power divider, two double balanced mixers and a quadrature hybrid. Generally, a phase equalized network that compensates for a differential phase length is included in the assembly.

From figure 2, it can be seen that two signals, of the same identical frequency and essentially the same amplitude, are applied to the unknown

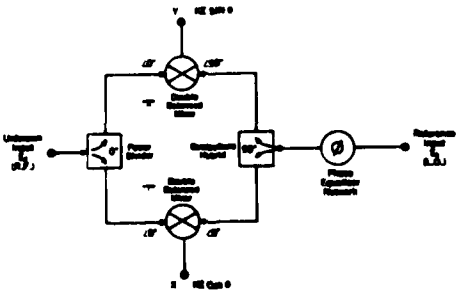


Figure 2. Block diagram of phase comparator.

RF and reference LO ports, respectively. These signals differ by electrical phase ϕ. The power divider splits the unknown signal into two equal amplitude/equal phase (0^0, 0^0) outputs.

The signal applied to the reference port is first phase equalized then split into two equal amplitudes, but quadrature (0^0, 90^0) phase outputs. Phase equalization is usually required to match the insertion phase characteristics of the quadrature hybrid with those of the power divider. Each mixer is therefore presented with two signals. When ϕ equals 0^0, double balanced mixer X is driven with two in-phase signals yielding a maximum positive voltage output; whereas mixer Y is driven with quadrature-phased signals yielding a zero voltage output. As ϕ is varied from 0^0 through 360^0, the output from the X mixer will vary as the COS ϕ and the Y as the SIN ϕ. Conversely, the phase difference between two signals can be determined by using the relationship:

$$\frac{E_y}{E_x}\phi = \text{arc tan} \tag{5}$$

(see Fig. 3).

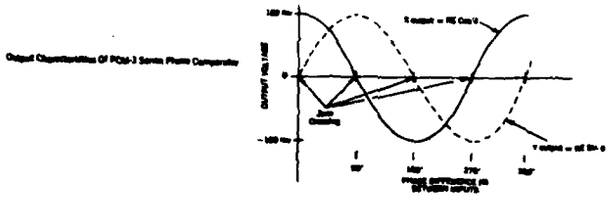


Figure 3. Output characteristics of phase comparator.

A phase comparator of this type exhibits a 3^0 error at center frequency. Error is the difference between measured outputs and the ideal outputs:

$$\phi_e = \phi m - \phi i \tag{6}$$

where ϕ_e is the phase error in electrical degrees, subscripts m and i are the measured and ideal values respectively.

The major causes of error are:

(1) Leakage signals - are signals from the Y path coupling to those in the X path. This source of error is minimized by proper location of the components and by using components of high isolation.

(2) Internal reflections and mismatch - these secondary signals may add, at all angles of phase, with mainstream signals thereby introducing phase perturbations. Using components with low VSWR minimizes this error.

(3) Mixer asymmetries - because the balanced mixers are used in pairs, any dissimilarities will generate errors. To minimize these errors, mixer pairs must be selected for extremely low direct coupled offset voltages and for close tracking of conversion loss.

(4) Phase equalization - while it is generally possible to completely equalize the insertion phase difference between the quadrature hybrid and the power divider at the design center frequency, it is almost impossible to achieve complete equalization over the entire bandwidth of the phase comparator.

Once the I and Q functions are derived, equation (2) must be implemented via digital or microcomputer hardware/software. The in-phase and quadrature signals, whose relative amplitude and polarity are a complex vector representation of the phase difference, are first digitized and translated into the required binary code[1]. The two signals are magnitude compared and checked for sign. The smaller number is shifted 8 bits and digitally divided by the larger number, the result forms the address of a look-up table in which the implementing equation (1) is to take the arc sin of ϕ which was just computed via either the look-up table or special purpose integrated circuit, e.g., AM 9511 or MM 6086.

For a microwave frequency of say 15 GHz, $\lambda = \frac{V_{light}}{f}$

$$\lambda = \frac{300 \times 10^6 \text{ M/S}}{15 \times 10^9} = 20 \times 10^{-3} = .02\text{M} = 0.78 \text{ in} \qquad (7)$$

$$\frac{\lambda}{2} = \frac{0.78 \text{ in}}{2} = 0.37 \text{ in.}$$

The wavelength is known at the particular RF center frequency. The baseline separation is fixed so $\frac{\lambda}{2\pi d}$ is a known number. Recall, from equation (1)

$$\theta = \frac{\lambda}{2\pi d} \sin^{-1} \phi. \qquad (8)$$

---

[1] Charles E. Konig and John T. Cervini, "Digital Phase Measurement Techniques," ERADCOM Tech Report DELEW-TR-80-4, December 1980.

Therefore, to implement the AOA calculation would require digitally multiplying the constant $\frac{\lambda}{2d}$ by arc sin ϕ. For instance, at 70 MHz,

$$\lambda = \frac{V \text{ light}}{f} = \frac{300 \times 10^6 \text{ m/s}}{70 \text{ MHz}} = 4.28 \text{ m} = 13.9 \text{ ft} \quad (9)$$

is required so that no ambiguity exists. To direction find on an emitter at 70 MHz would require a baseline of at least

$$\frac{D}{2} \text{ or } \frac{13.9}{2} = 6.96 \quad (10)$$

or approximately seven feet antenna separation. This means with an antenna spacing of approximately seven feet, no ambiguities can exist in this particular DF system. Thus the phase, frequency and AOA will be unambiguous.

b. Receiver Description

A state-of-the art dual channel surface acoustic wave (SAW) compressive receiver was designed and built.[2] This receiver represents a technical breakthrough in a fast scanning phase-preserving receiver system (see Fig. 4). This type of receiver can be used for narrowband UHF work or as an intermediate frequency (IF) for a broadband microwave receiver.

Channels 1 and 2 are fed with identical but phase shifted signals similar to those obtained by connecting the channels to individual, spatially separated antennas. The chirp waveform required to multiply their port signals is generated by impulsing an up-chirping SAW pulse compression line (PCL). This chirp PCL 1, expands the impulse source into a linear frequency modulation (FM) sweeping signal, which multiplies the input signals on both processor channels. The PCL 2 matched filters perform the actual transform processing and outputs the signal spectrum components as a series of RF pulses, at a repetition rate which is in synchronization with the pulse rate of the SAW's.

The dual channel SAW receiver IF processor implemented has a limited dynamic range in its present configuration of 15 dB, and a measured input signal level sensitivity of -10 dBm. The receivers dynamic range can be improved with a high quality mixer or multiplier circuit plus a limiter amplifier, and sensitivity can be improved with a phase comparator whose input drive level is lower.

Figure 5 shows the input pulse required to excite the SAW filters.[3] Its pulse width is 10 ns (nanoseconds) and its pulse period is 1 μs (microseconds).

---

[2] D. R. Klose and W. J. Skudera, "Dual-Channel SAW Compressive Direction-Finding Techniques," Army Science Conference Proceedings, Vol 4, pg 95-110, June 1980.

[3] W. Skudera, "The Versatility of The 'In-Line' SAW Chirp Filters," Proceedings of the 31st Annual Frequency Control Symposium, pg 286, June 1977.

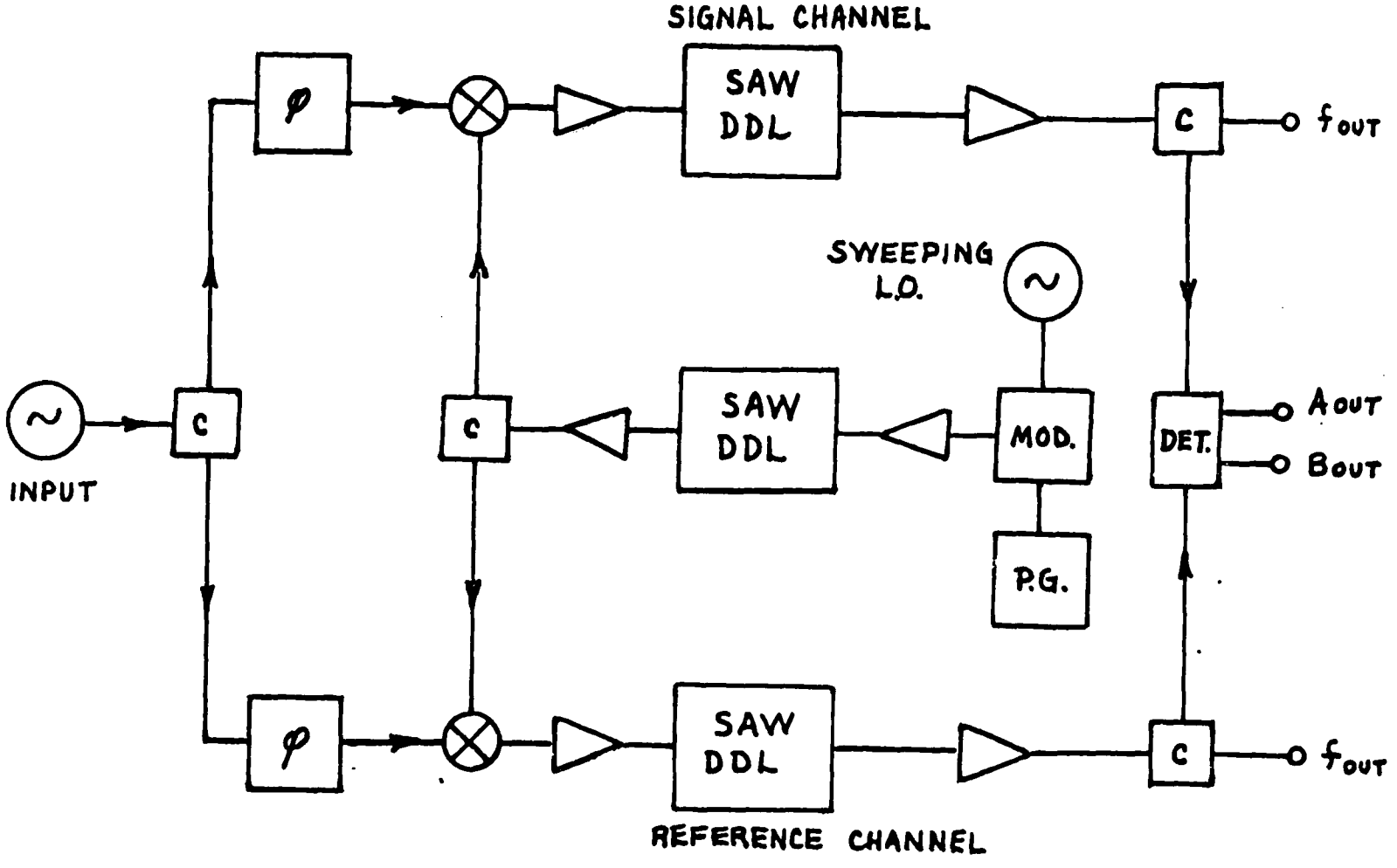


Figure 4. Dual channel SAW receiver block diagram.

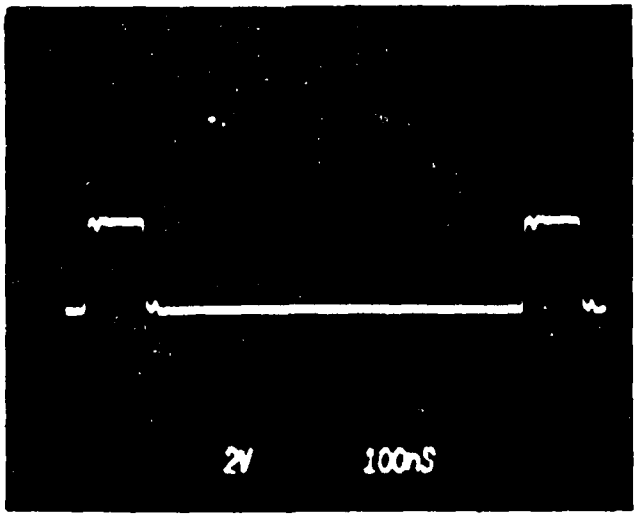


Figure 5. Input pulse for SAW filters.

Figure 6 illustrates the frequency phase characteristics of the receiver. The top trace is the RF signal output and the bottom is one channel of undetected phase.

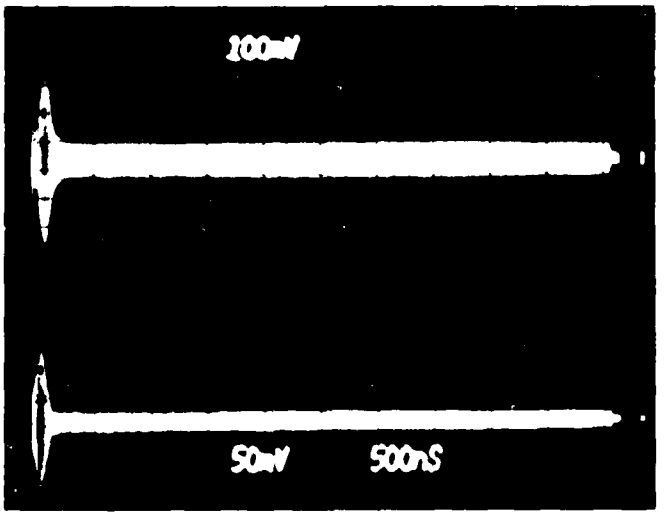


Figure 6. Frequency/phase output characteristic of SAW receiver.

Figure 7 illustrates both phase channel and video detected.

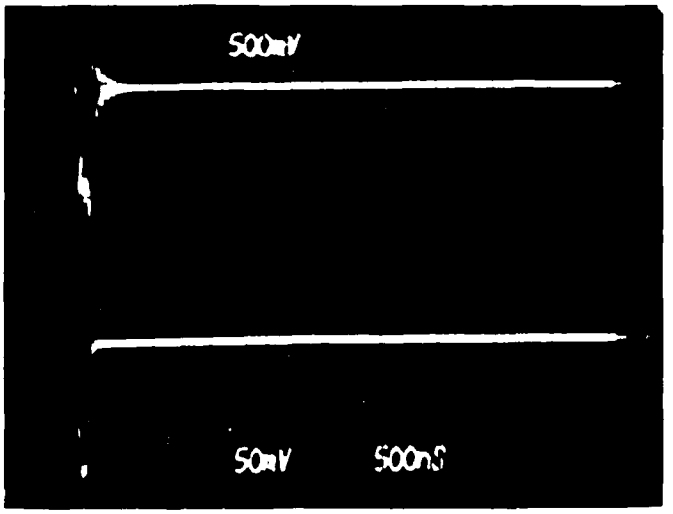


Figure 7. Video detected phase outputs.

Figure 8 shows the instrumentation needed to test and operate the dual channel SAW receiver. One Wavetek generator acts as the LO for the chirp and the other Wavetek generator simulates the RF signal input. The high frequency pulse generator is used to trigger the SAW filters. A Tektronix oscilloscope Model 7904 is used to display the frequency and phase information.

Currently, the SAW receiver has a throughput of 1 MHz but data rates as high as 4 MHz can be achieved. Its bandwidth is limited to 10 MHz at this center frequency but bandwidths of 500 MHz can be realized. The mainstay of the SAW's receiver are its three filters; which are a combination of the transversal and the SAW filters.

Transversal filters use time delays instead of a feedback network of resonances. The signal enters the delays D which are set in magnitude by attenuators A. When the path outputs are summed, the passband frequencies add and the rejection band frequencies cancel. Consequently transversal filters are best understood in the time domain (see Fig. 9).

In a SAW filter a piezoelectric substrate (like quartz) holds two transducers, each constructed of a network of electrodes or fingers. The spacing between the fingers equate to the time delay D of the transversal filter. The input signal perturbs the piezoelectric substrated to launch an acoustic wave. Energy is launched only where a finger pair overlaps and that overlap equates to the weighting A. After the wave travels the length of the crystal, a reverse process reconverts it to a voltage (see Fig. 10).

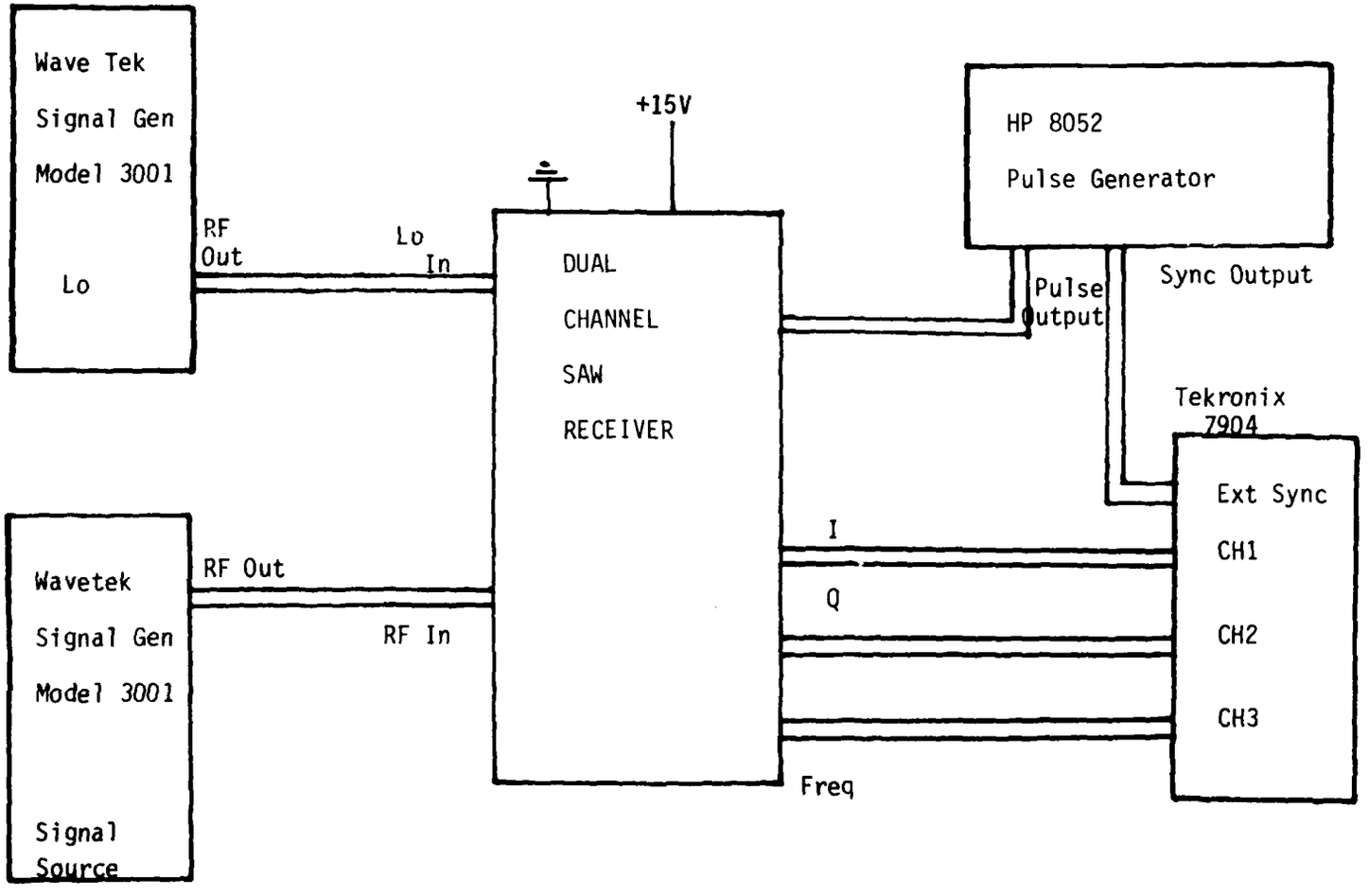


Figure 8. Receiver instrumentation.

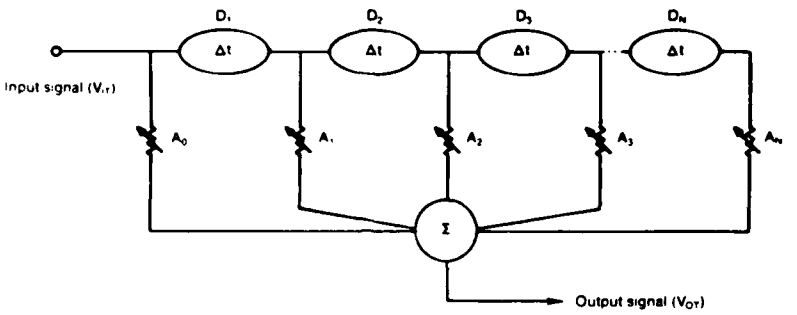


Figure 9. Transversal filters time delay diagram.

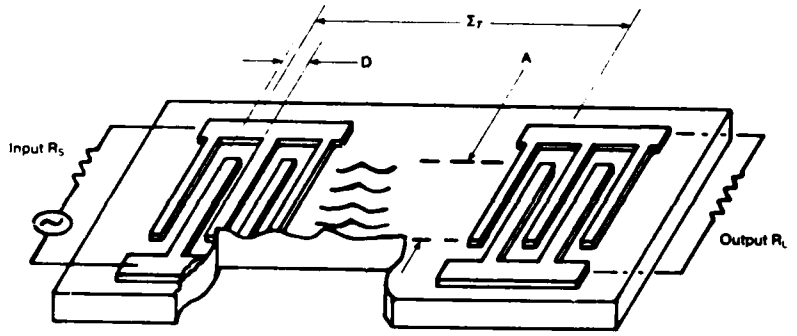


Figure 10. SAW filters piezoelectric substrate.

The delay response of a 15 tap transversal filter with equal delay D and uniform attenuation (weighting) A, in each leg (a), yields a sinf/f frequency response (b) (see Fig. 11). The 4 dB bandwidth equals the inverse of the total filter delay. As the required bandwidth narrows, total delay and the filters physical size must increase. Also, the first sidelobes of the response are only 13 dB below the main lobe.

Non-uniform (apodized) weighting (a) produces a more desirable rectangular frequency response (b), and improves rejection to 50 dB or better (see Fig. 12). In the transversal filter the delays and the weighting are pure, real numbers. The absence of poles leads to a linear phase characteristic.

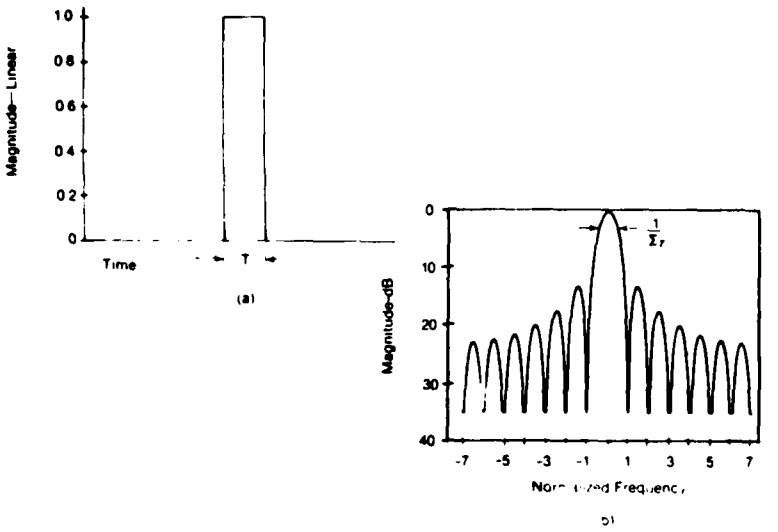


Figure 11. Delay response of a 15 tap filter.

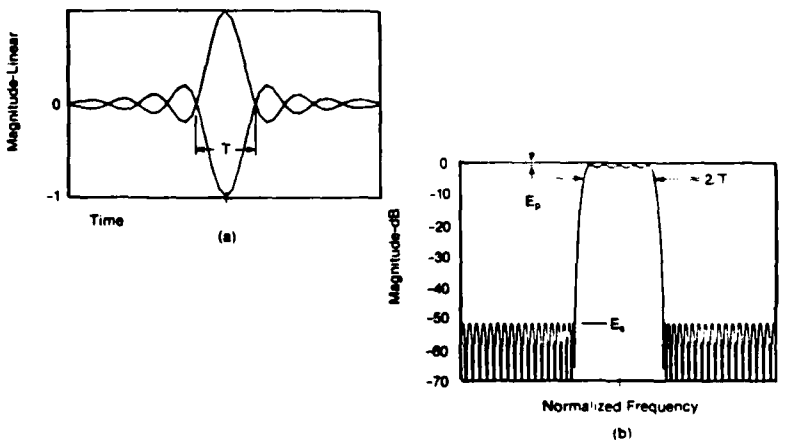


Figure 12. Non-uniform weighting.

Key SAW filter parameters and practical performance ranges are defined in Table 1.

TABLE 1. KEY PARAMETERS AND PRACTICAL PERFORMANCE RANGES

Definition	Symbol	Range
Center Frequency	f_o	10 to 1000 MHz
Bandwidth @ 1 dB	Δf	0.06 MHz to 40% f_o
Rejection bandwidth @R db	Δfr	Δ+ 0.7 MHz
Transition width	f_t	0.35 MHz to 2 MHz
Shape factor	SF	1.04:1 to $\frac{\Delta f + 4 \text{ MHz}}{\Delta f}$
Amplitude ripple	AR	+ 0.3 dB
Insertion loss	IL	6 to 30 dB
Ultimate rejection	R	45 dB
Peak phase deviation (from linearity)	$\Delta\phi$	$+3^o$

The practical range of center frequency and bandwidth (10 MHz < f_o < 1000 MHz) for commercial SAW filters is restricted on the lower limit by bulk waves and other spurious responses, and on the upper limit by the line (finger) resolution. Generally, the width of the fingers and the space between them are made equal. When the fingers are spaced by a quarter wavelength, outputs are produced at the fundamental design frequency and at the third and the fifth harmonics. Line widths (LW) are calculated by

$$LW = V/8\ f_o \qquad (11)$$

f_o = center frequency

V = velocity of material.

Designs are sometimes optimized at a harmonic for higher frequency performance. Such designs have been successful above 1 GHz (see Fig. 13).

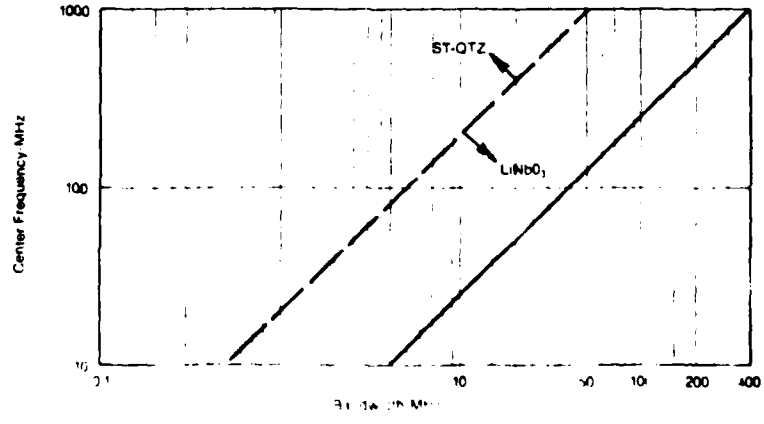


Figure 13. Practical frequency and bandwidth of SAW filters.

The minimum insertion loss of a two transducer SAW filter is shown as a function of fractional bandwidth for different substrates. The (b) directional input transducer dictates the 6 dB loss (see Fig. 14). The shape factors that can be achieved for SAW filters are determined by the number of wavelengths < N (40 < N < 400) (see Fig. 15).

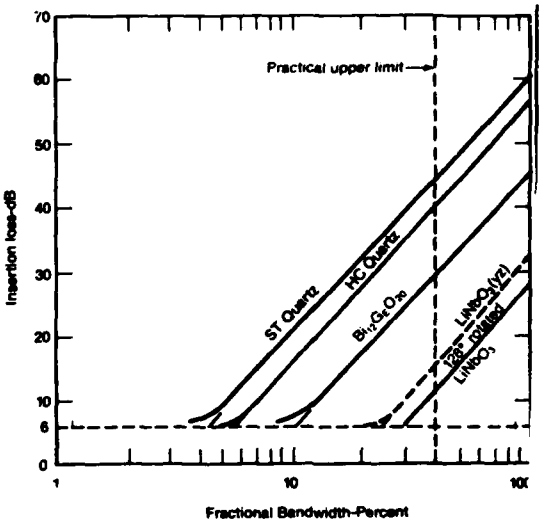


Figure 14. Fractional bandwidths for various substrates.

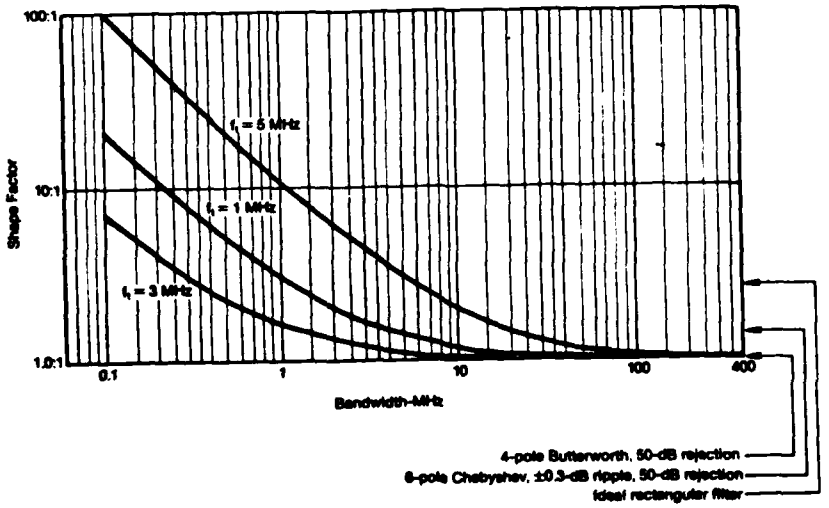


Figure 15. Shape factor versus bandwidth.

The practical bandwidth range of SAW filters is 0.1% to 40% of center frequency, with a lower limit of 60 kHz. For more narrow bandwidths, the transducer requires an excessive number of fingers, and unwanted reflections will dominate and degrade its performance. For larger bandwidths, too few fingers are used and the response becomes distorted.

Tuning a SAW filter begins with the selection of an impedance matching network with good temperature stability that compromises loss, distortion and spurious response. Although loss must be minimized so must phase and amplitude distortion. Tightly tuning the filter will increase spurious distortion and some degree of mismatch may actually be desired.

c. SAW CHIRP Transversal Filter

Surface waves can be generated when metal electrodes are spaced a half wavelength apart on a polished piezoelectric substrate and driven 180^0 out of phase. One set of synchronous electrodes can be used to form an input transducer located on one end of the substrate, and a second set of synchronous electrodes can be used to form an output transducer located on the opposite end of the substrate. This type of arrangement is used to create a fixed delay line since all the electrodes are equally spaced. Dispersive delay lines or chirp filters are fabricated similarly to the fixed surface wave delay lines but with the exception that the spacing between the electrodes are not held constant; instead, they have a graded periodicity design.[4] The graded periodicity permits each elecrode pair to be synchronous at a different fixed frequency and, because the physical position of each electrode pair is different, the time delay will vary with frequency since the delay time equals distance divided by the acoustic velocity.[5,6] As a result the input transducer becomes dispersive and, if the output transducer has the same slope, that is, high frequencies traveling the shortest distance with low frequencies traveling the longest distance, then the dispersion is doubled. This type of arrangement is called a down chirp pattern because the delay versus frequency slope is negative. If the input and output transducers are interchanged, then this type of arrangement is called an up chirp pattern because the dispersion (T) is positive. In practice one impulses the input transducer and an expanded RF time signal is received at the output transducer.

d. Analog Interface

The analog interface is needed to marry the SAW receiver with the digital logic processing section. The interface block diagram is shown in figure 16 and consists primarily of 5 HP pulse amplifiers and a video detector. Each amplifier has a gain of 40 dB and an input/output impedance of 50 ohm. The amplifiers have a rise time of less than 4 μs and a noise level of less than 40 μV. A total gain of 80 dB is required on each phase channel. Figure 17 illustrates the amplified phase signals.

[4] W. J. Skudera and H. M. Gerard, "Some Practical Considerations of Dispersive Surface Wave Filters," Proceedings of the 27th Annual Symposium on Frequency Control, pg 253-261, June 1973.

[5] W. J. Skudera and G. LeMeune, "Acoustic Surface Wave Fabrication Techniques and Results," ECOM Technical Report 4333, August 1975.

[6] W. J. Skudera and G. LeMeune, "A 70 MHz Surface Wave Chirp Filter," presented to the Communictions Research Technical Area, COMM/ADP, July 1975.

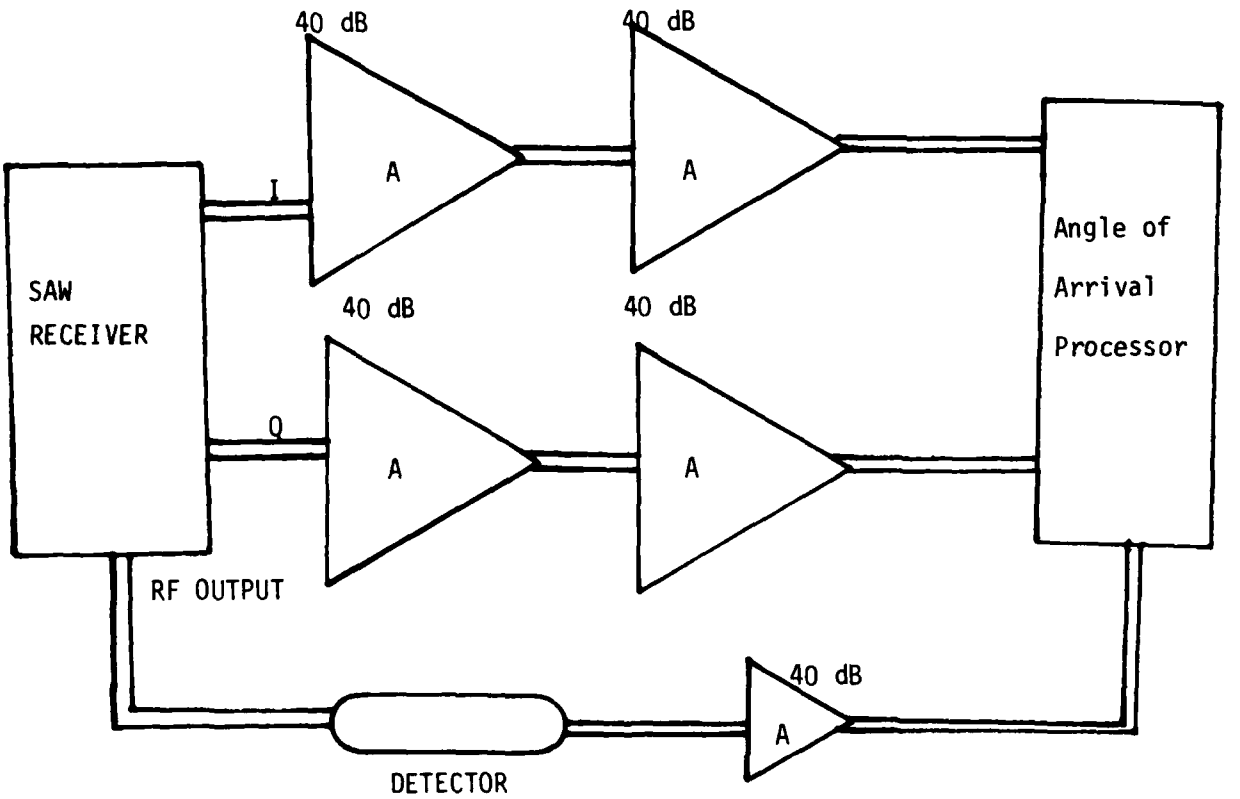


Figure 16. Block diagram of interface.

The pulsed RF output on the frequency channel is first video detected and then amplified. A 50 ohm cable is used throughout the interface connections. The amplified phase and frequency data are digitized via a flash analog-to-digital (A/D) converter. It is considered desirable to associate the phase angle with the frequency of operation for clearer emitter identification. More importantly, AOA and frequency must be "carried" along through the digital processor with the same pipeline delay.

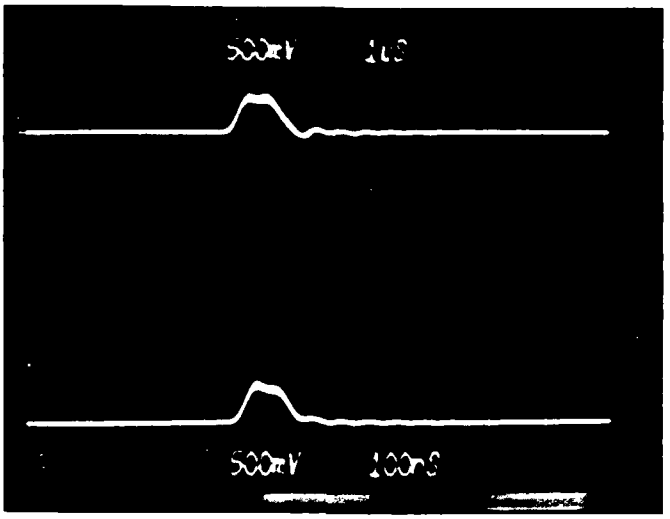


Figure 17. Amplified I, Q outputs.

There are several considerations concerning the interface. First, the noise levels on the phase channels have to be measured and filtered. Figure 18 illustrates RF noise riding on top of one channel of phase angle sweep output. Figure 19 shows the same sweep with a 20 MHz bandwidth scope filter. Notice a significant reduction in distortion as well as a 30mV reduction in noise level. Second, a low pass filter with a cut-off of 20 MHz inserted before the amplifiers is required to remove harmonic mixing intermodulation products as well as RF feed-through.

In order to optimize output voltage levels for A/D conversion, the receiver is not optimized for minimum distortion. For maximum phase angle sweep, the input levels on the signal and LO insert are altered. Ideally, the interface requires a video amplifier with variable gain and a low noise figure. Figure 17 shows the two amplified video phase channels connected to the A/D converters with a gain of 65 dB. Since there is a slight mismatch - 50 ohm line looking into the 80 ohm input of the A/D converter - the resulting reflection produces a rounding to the video pulse.

One big problem that had to be resolved was the timing between the receiver sweep pulses to excite the SAW filters and the start conversion pulse of the A/D converters. The current design of the SAW devices cannot be pulsed at more than a one μs repetition rate. This limits the receiver throughput.

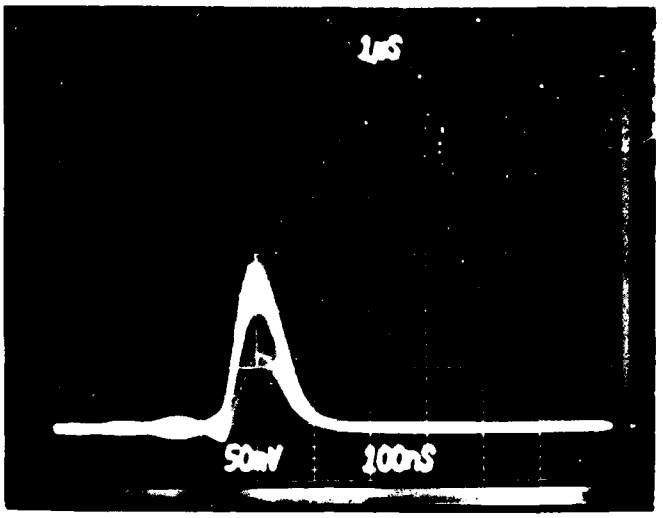


Figure 18. Phase output before filtering.

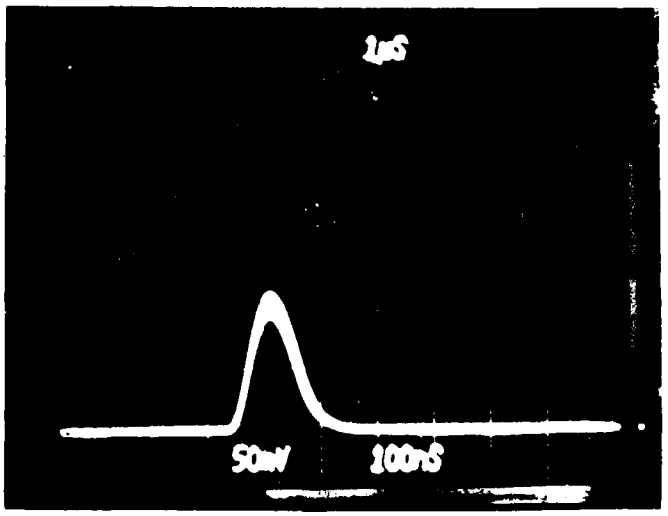


Figure 19. Phase output with 20 MHz filter.

The A/D converter's START conversion pulse must be in synchronism with the SAW's exciter pulse. Therefore, the repetition rate or the pulse output for the receiver is externally synchronized by the A/D convert pulse (see Fig. 20). The external input on the HP 8015A accepts a +7V dc input. The repetition rate is now externally controlled and in synchronization with the receiver, but the pulse width is externally controlled by the vernier on the generator.

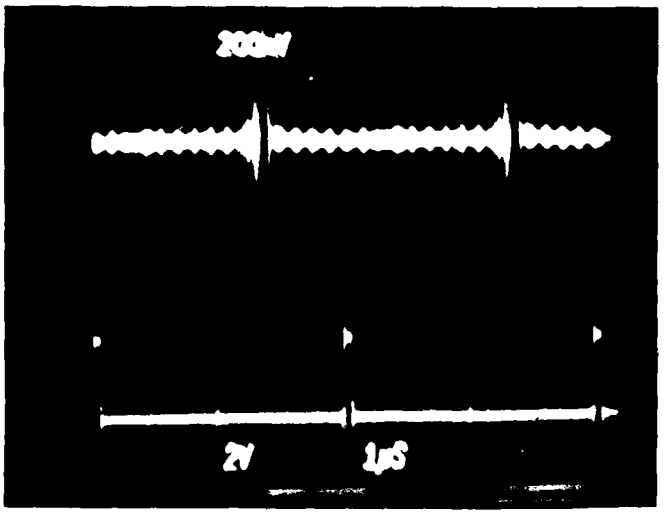


Figure 20. Receiver output plus A/D strobe.

As can be seen in figure 20, it is clear that the master trigger must originate from the slow chirp pulse and will require a phase lock loop to synchronize the master clock; or a delayed trigger pulse from the master clock.

Figure 21 shows the A/D converter sample pulse (bottom trace) in synchronism with the receiver output RF pulser (top trace). Notice the widening of the RF pulse. This is due to sweeping the SAW filters too fast. Looking at figure 22, the same signals are photographed but at a slower repetition rate. Notice the sharp peaks on the IF output.

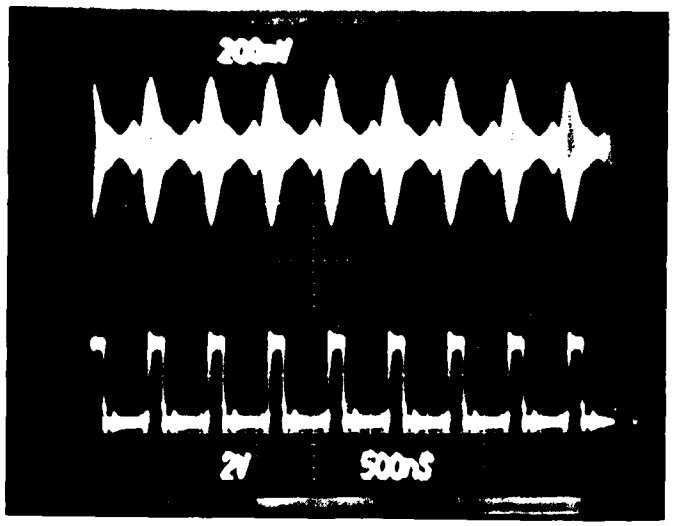


Figure 21. Receiver RF output plus A/D convert pulse.

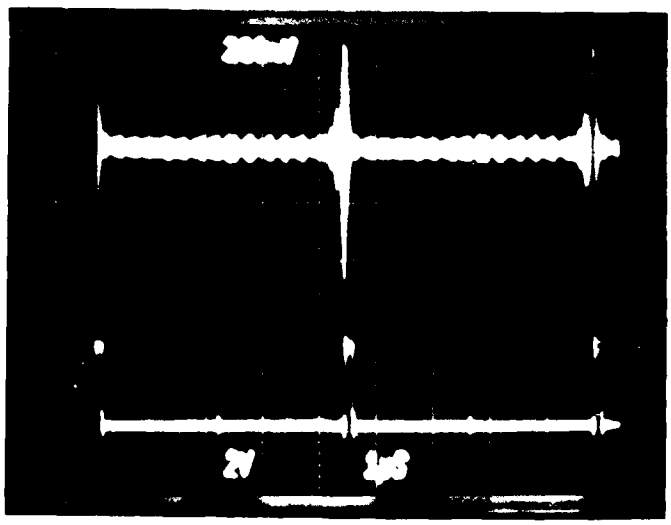


Figure 22. Receiver output unsynchronized.

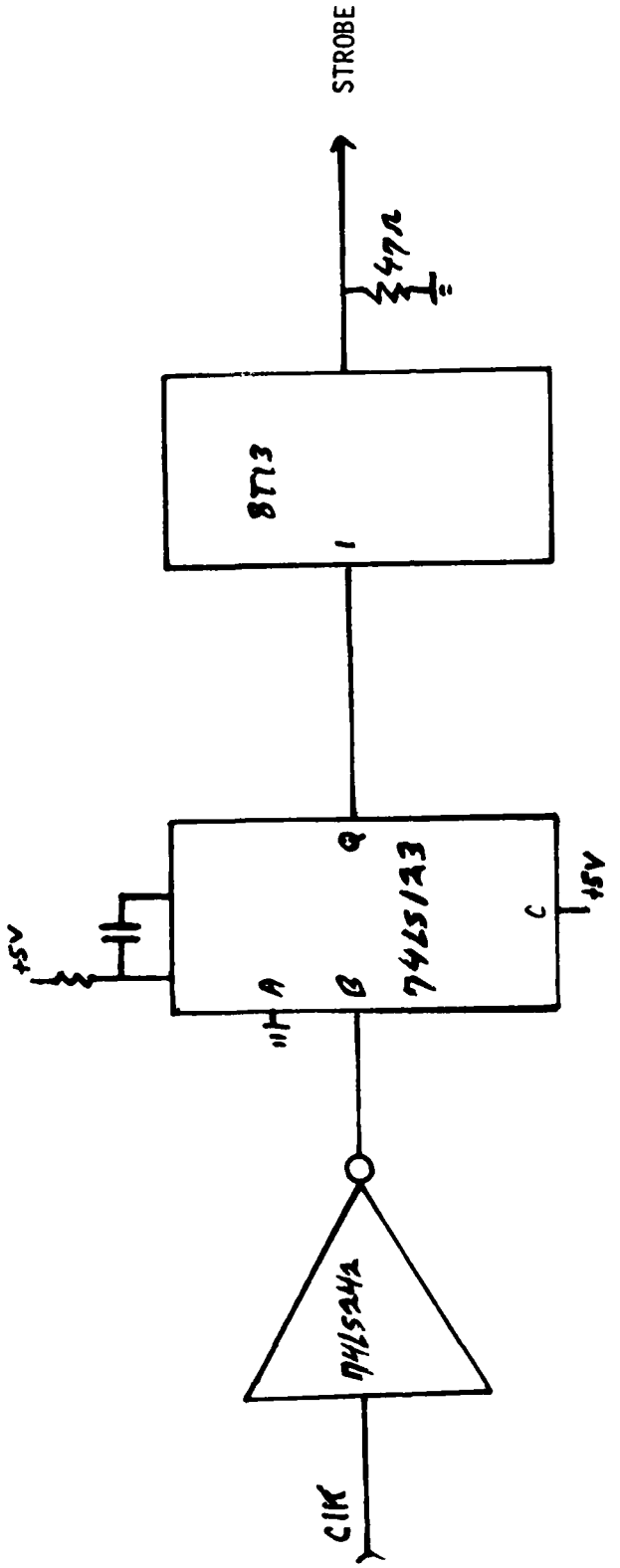


Figure 23. Sample pulse for A/D converter.

e. Digital Processing Section

The phase angle measurement and calculation for a phase interferometer was discussed at length in report, "Digital Phase Measurement Techniques," DELEW-TR-80-4, December 1980, by Konig and Cervini.[1] The subsequent redesign and improvement of such a system will be described. The major design change was generating all the timing and control signals from a master clock. The analog to digital converter, convert pulse circuit, was redesigned and is shown in figure 23.

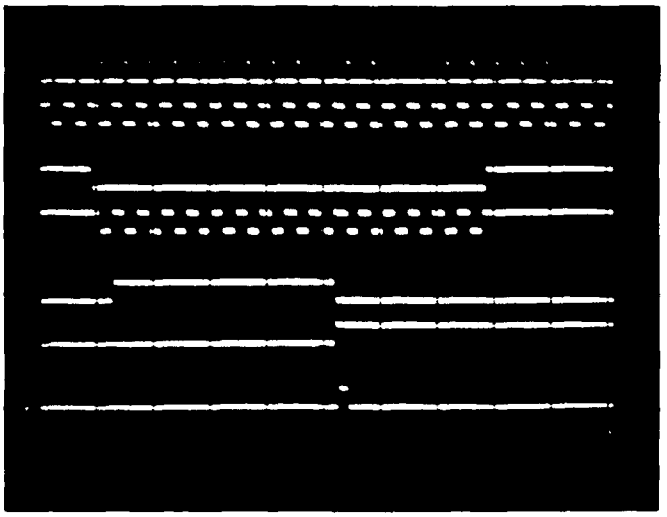


Figure 24. System timing and control signals.

The circuit consists of an inverting buffer AM25LS242, a one shot multivibrator 74LS123 and a line driver 8T13. On a rising edge of the clock pulse, the one shot puts out a pulse with a width of 50 ns and duty cycle of 1 μs.

The timing for this digital system must be derived from a clock of known pulse period and pulse repetition rate. Since the analog to digital converter is the first component in any digital system it must be controlled or in synchronization with the master clock. This digital system requires that the A/D converter be sampled every 1 μs with a 50 ns convert pulse. This pulse train is derived from a retriggerable monostable multivibrator. It features direct coupled triggering from high level inputs. Complementary outputs are provided. A fan-out of 10 transistor-transistor logic (TTL) loads is available from each output. A TTL load is a circuit which can sink 8 mA and source 40 uA.

[1]Konig & Cervini loc. cit.

A one shot triggers the $\overline{CLK}$ because it needs to sample an A/D converter just before WRITE/READ (WE) signals go into a READ state. Since the one shot pulse has to drive two A/D converters with a combined impedance of 40 ohm, a line driver was included in the circuitry.

Figure 24 shows all the timing and control signals associated with the A/D circuitry. The timing and control circuit, for the code conversion board, is shown in figure 25.

The WE clock has to be generated from the $\overline{CLK}$ because the 8291 binary counter triggers on a down step. A timing WE cycle (pipe line delay) on the order of 32 μs is generated. This circuit consists of a divide down by 16 which feeds to the WE line of a two port bipolar RAM. This circuit provides both the WE and $\overline{WE}$ signals. The circuit consists of a presetable binary 8291 counter and a D-type flip flop 7474. The flip flop takes the divide by 16 counter output and divides by two. The resultant divide by 32, provides a WRITE of 16 μs and a READ of 16 μs, and has a pipeline delay of 32 μs. Clock triggering of the 7474 occurs at the voltage level of the clock pulse and voltage at the transition time of the positive going pulse.

The timing for the sign magnitude board's operation is basically synchronous except for a clock to latch the registers. All other circuitry is a function of the propagation delays and RC time constants of the interconnect wiring. It is the fastest board and has virtually no delays associated with it. Clock is used instead of $\overline{CLK}$ because the circuit is running so fast that a half cycle change has no effect on the board's performance.

The timing for divide board is shown in figure 26. The divide board is the heart of the system and the reason for the RAM buffers. The divide takes eight clock cycles which imposes a requirement on the buffer memory of a long pipeline delay. A Nand gate only lets the $\overline{CLK}$ signal clock the SAR AM 2503. When the RAM buffers are in the READ state, a division takes place only in the READ mode in which the data R, I are completely stable and no error can exist.

The conversion complete (CC) signal, therefore, stays low and only goes high again when the WE line is high. A one shot rests the successive approximation register (SAR) and CC stays low until the clock is active again, i.e., when WE is low.

Phase Angle Look-up is the resultant output from the division, i.e., quotient is the address for a look-up table. In the look-up table is the electrical phase angle which is derived from the in-phase and quadrature components of the signal. Table 2 shows reasonably good agreement over the operating range of the PROM.

Angles from 0^{o} to 90^{o} in electrical phase can be resolved. The AOA is now computed (see Fig. 27 and equation (1)). The phase angle forms an address whose ARC SIN is stored in read only memory (ROM). This angle is then multiplied by a constant K to compute the final AOA. The constant K is a function of frequency and antenna separation.

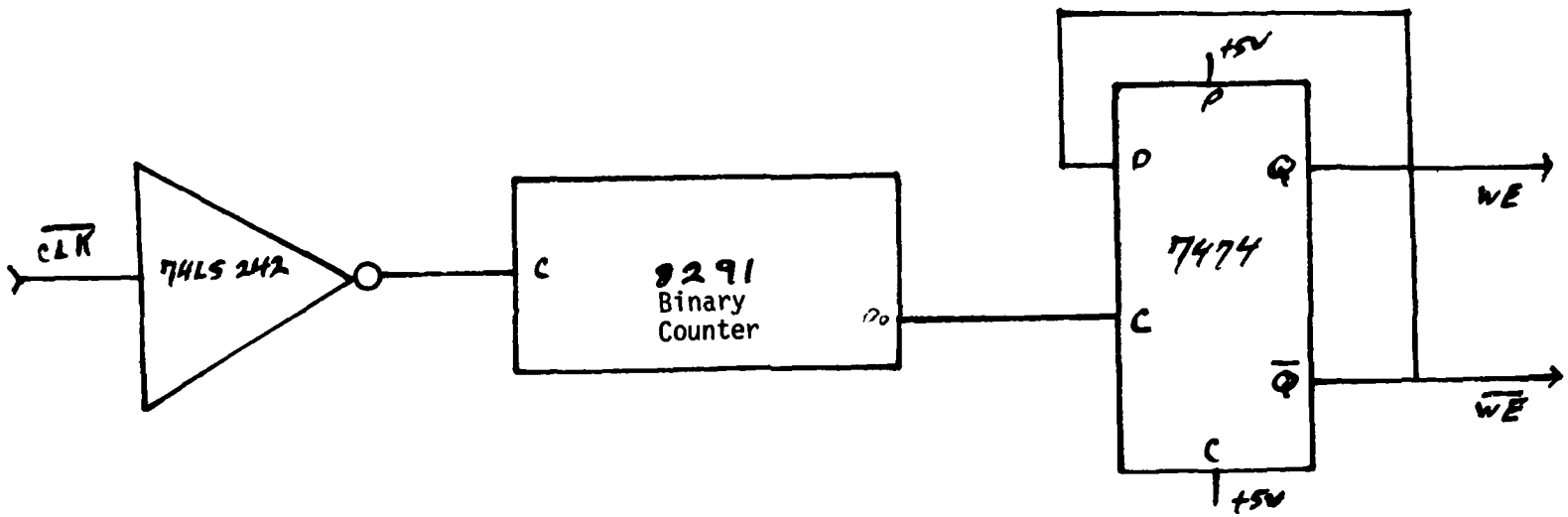


Figure 25. Timing for code conversion board.

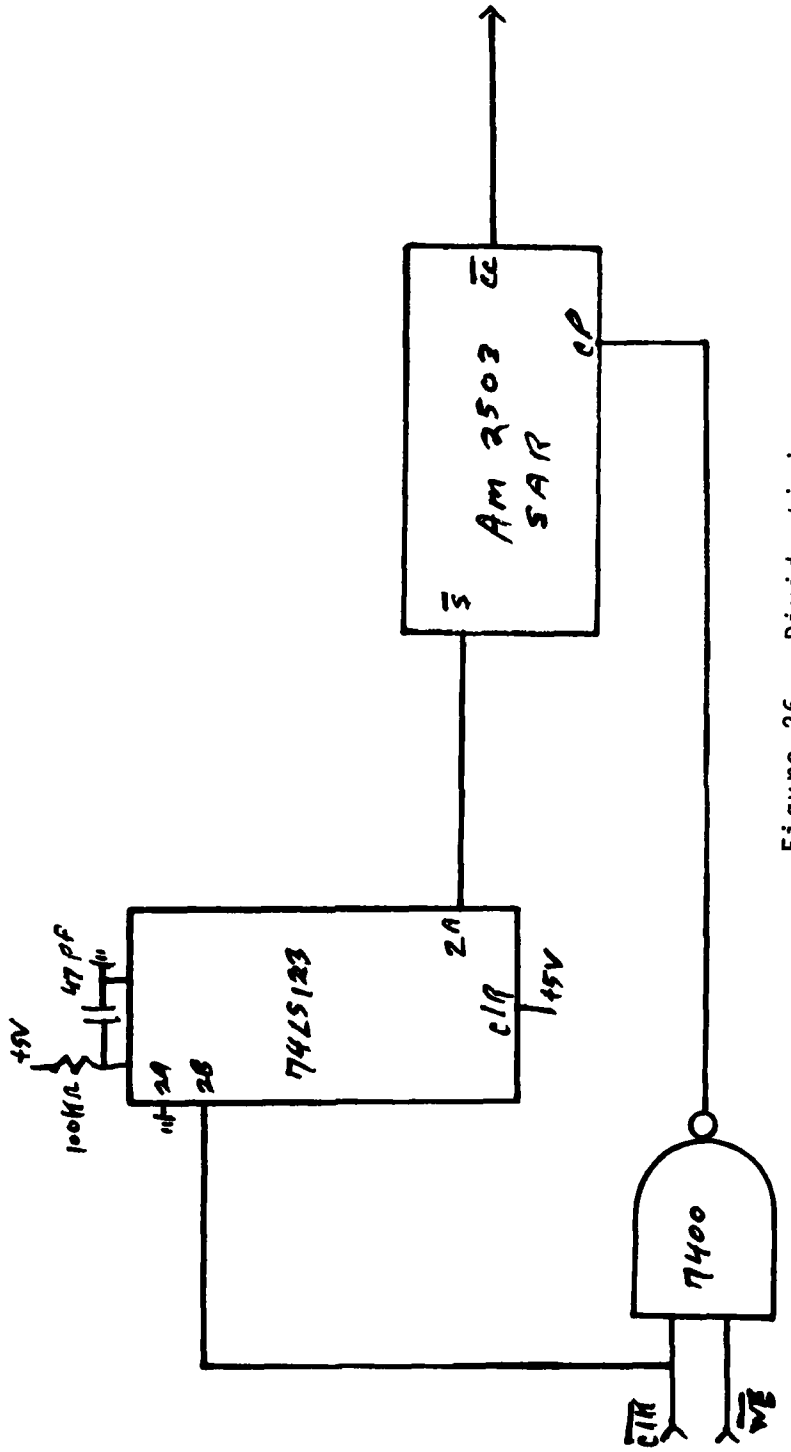


Figure 26. Divide timing.

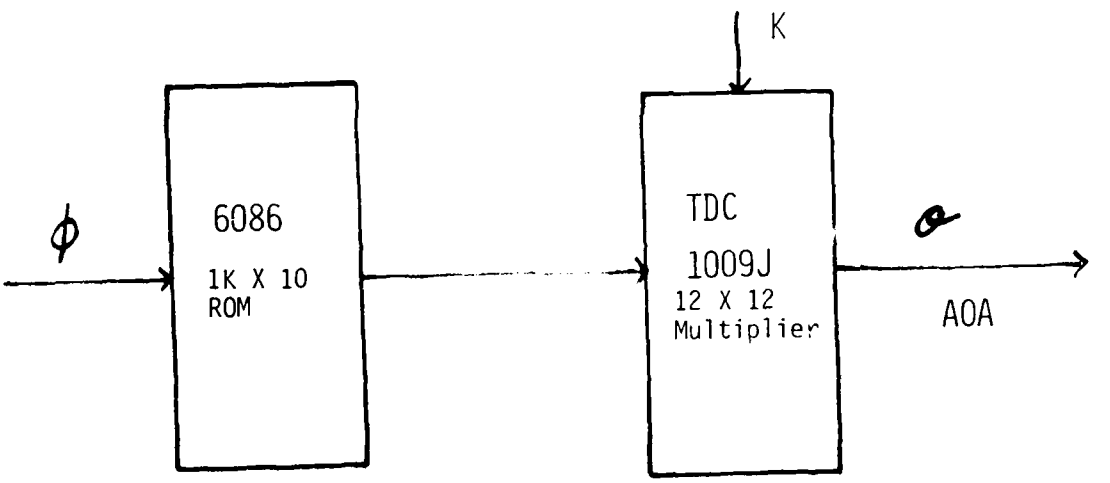


Figure 27. AOA Calculation circuit.

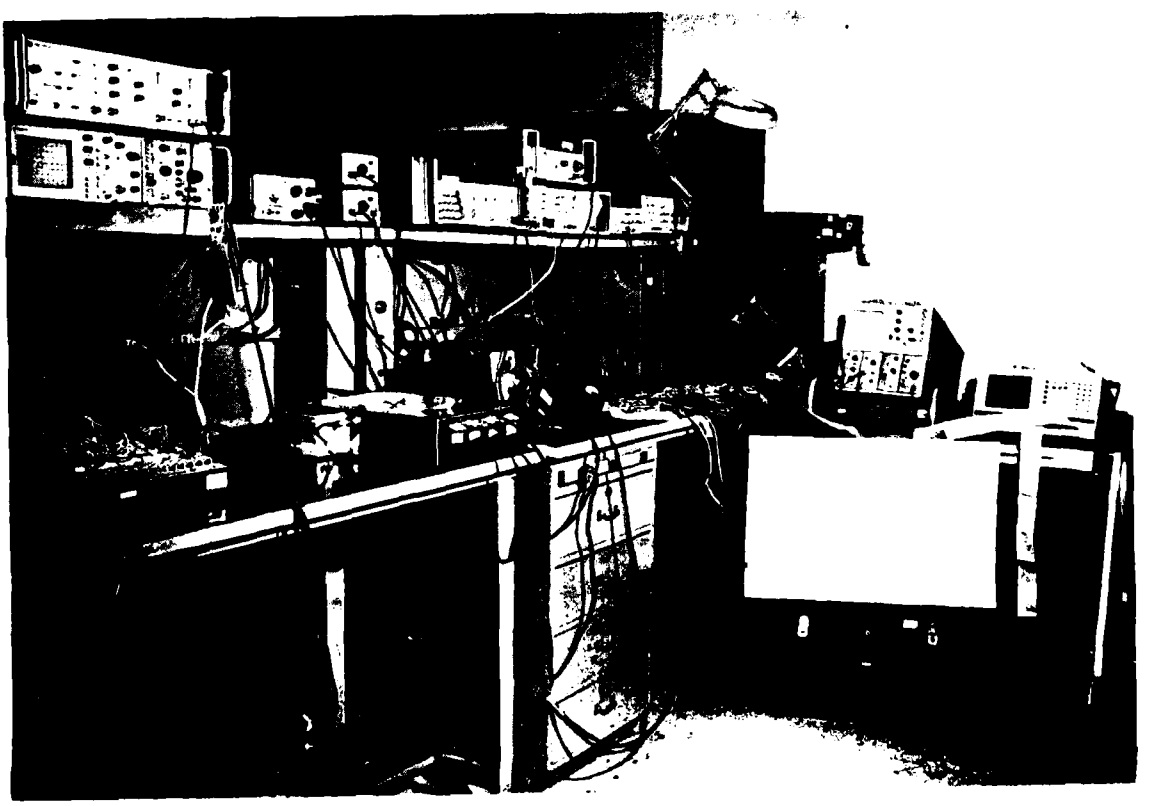


Figure 28. Phase interferometer test bed.

TABLE 2. PHASE ANGLE MEASUREMENTS

COS (mv)	SIN (mv)	THEO (angle)	Actual (angle)
0	500	45	45
50	490	40	36
120	485	30	33
190	460	22	28
145	480	28	27
170	470	25	25
280	420	12	16

Note the errors due to approximately fifty millivolts of noise on phase angle signals and a reading error because of the voltage measurements made by eyeballing the oscilloscope.

The Monolithic Memory 6086 (1024 words by 10 bit ROM) has been customized to make a SIN look-up table for 0^{o} - 90^{o}. The address inputs are used to quadrant the angles in increments to 0.09^{o}. The 10 bit output code has not been rounded so that the output error is 0.0009.

TRW multiplier/accumulator Model TDC 1009J is a very high speed TTL compatible device. It is a 12 X 12 parallel array multiplier with double precision or rounded outputs. The SIN look-up and multiply take a lightning fast 215 ns.

The entire AOA calculation minus the pipeline delay has the capability of running at 600 ns. This means monopulse radar signals can be processed at a 1.7 million pulse per second rate.

CONCLUSIONS/RECOMMENDATIONS

The processor described in this report illustrates the major portion of analog, RF, digital components and circuitry required to implement a realtime monopulse AOA receiver direction finder.

To completely implement this processor the following conclusions are noted:

a. A digital synchronous circuit driven by the SAW sweeping LO is needed to properly trigger the A/D circuit.

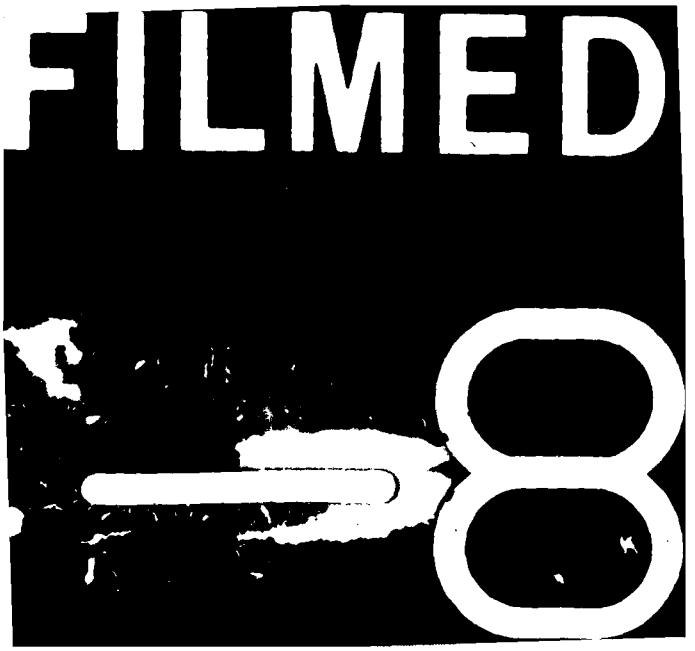
b. A digital circuit is needed so that the PROMS can output over a full 90^{o} range.

c. Some development work on the phase discriminator is needed to yield a larger output voltage sweeping per differential phase shift.

The next major phase of this program will be to design and construct a wideband microwave front-end with a 2-4 GHz baseband.

List of Acronyms

AOA	angle of arrival
DF	direction finding
EW	electronic warfare
FM	frequency modulation
IF	intermediate frequency
LO	local oscillator
LOB	line-of-bearing
LW	line width
PCL	pulse compression line
RF	radio freqeuncy
ROM	read only memory
SAW	surface acoustic wave
TTL	transistor transistor logic
VSWR	voltage standing wave ratio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